DO NOT ENTER TLW 08/28/2007

Listing of the Claims

1. (Currently Amended) A method comprising:

   in a processor based system where a plurality of processors manage and share processor execution resources in hardware, in response to a first processor in the plurality of processors being scheduled to enter an idle state, making a processor execution resource previously reserved for the first processor available to a second processor in the plurality of processors.

2. (Original) The method of claim 1 further comprising reserving the processor execution resource for the first processor in response to the first processor being scheduled to execute a task.

3. (Original) The method of claim 2 wherein each of the plurality of processors is a logical processor of the processor based system.

4. (Original) The method of claim 3 wherein the first processor being scheduled to enter an idle state further comprises the first processor executing a processor instruction requesting the first processor to enter an idle state.

5. (Original) The method of claim 4 wherein making the processor execution resource previously reserved for the first processor available to a second processor further comprises releasing the processor execution resource into a common pool of processor execution resources accessible from the second processor.

6. (Original) The method of claim 5 wherein the first processor being scheduled to execute a task further comprises the first processor receiving a wake up signal.